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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,769	05/14/2001	Takashi Hotta	500.28166CX2	7218

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,769	HOTTA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/24/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-40 (claims 1-16 have been canceled)* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/433,368.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-16 have been canceled. Claims 17-40 are presented for examination. Claim 26 of the first occurrence is assumed to be claim 22. Correction by applicant is kindly suggested. Claims 17-40 were apparently not available at the time of examination. In order to give applicant a chance to respond , the following is a non-final action based on a new ground

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 17-40 are rejected under 35 U.S.C. 102(a) as being anticipated by DeGroot (4,766,564).

3. As to claims 17,18, 23-25, DeGroot disclosed a system including at least :

a) a register for storing data (see fig.1);

b) a plurality of arithmetic operation units to execute plurality of instructions stored in memory in parallel (see fig.1, ADD, MUL);

c) a plurality of signal lines for sending data stored in the register to an arithmetic unit (see the output connection 22,24 of the register to the input of ADD and MUL in fig.1);

d) a second plurality of signal lines for storing result data from the arithmetic units in register (see output of ADD and MUL to the input of register in fig.1);

e) a bypass circuit (adder bypass bus and mul bypass bus) for connecting the first and second plurality of signal lines to use data resulting from the arithmetic output for next cycle (see fig.1, see the bypass bus with the switches from the arithmetic units to the input of the arithmetic units), the bypass being controlled by instructions(see the control of arithmetic instructions in col.3, lines 1-46, see fig.3, see also col.5, lines 17-42 for bypass cycle).

4. As to claims 19, 20, DeGroot also included switches (see the switches in fig.3).

5. As to claim 21 , 22 (26 by applicant) DeGroot disclosed a system including at least :

a) a register for storing data (see fig.1);

b) a plurality of arithmetic operation units to execute plurality of instructions stored in memory in parallel (see fig.1, ADD, MUL);

c) a plurality of signal lines for sending data stored in the register to an arithmetic unit (see the output connection 22,24 of the register to the input of ADD and MUL in fig.1);

d) a second plurality of signal lines for storing result data from the arithmetic units in register (see output of ADD and MUL to the input of register in fig.1);

e) a plurality of switches (see the switches with the adder bypass bus and mul bypass bus in fig.3) for connecting the first and second plurality of signal lines to use data resulting from the arithmetic output for next cycle (see fig.1, see the bypass bus with the switches from the arithmetic units to the input of the arithmetic units), the bypass

being controlled by instructions(see the control of arithmetic instructions in col.3, lines 1-46, see fig.3).

6. As to claim 26 (second claim 26 by applicant) , DeGroot also included different arithmetic operations (see the ADD and MUL in fig.3).

7. As to claims 27,28,29,30, 31-34, DeGroot also included bypass for transferring the data between the different arithmetic units (see the input connection to the switch at each input of the arithmetic units in fig.3, see also limitations already set forth in paragraph # 3 and 5).

8. As to claims 35,36, DeGroot also included bypass for transferring the data between the different arithmetic units and also into the register (see the input connection to both the register input and to the switch at each input of the arithmetic units in fig.3, see also limitations already set forth in paragraph #).

9. As to claim 37, DeGroot also included at least :

a) a plurality of registers (see the register file);

b) first and second arithmetic units for execution instructions based on plurality of instructions stored in memory (see the execution of the arithmetic instructions in col.3, lines 5-46);

c) firs t signal lines transferring data from registers to the first arithmetic unit (see the output 22 from the register to the ADD);

d) second signal lines transferring data from registers to second arithmetic unit (see the output 24 from registers ton the MUL in fig.3);

e) third signal fro transferring data from the first arithmetic unit [ADD} to the register (see output from ADD into registers 8 in fig.1);

f) fourth signal fro transferring data from the second arithmetic unit [MUL] to the register (see output from MUL into registers 8 in fig.1);

g) the first bypass bus (see fig1 , the bypass to the input switch of ADD);

h) the second bypass bus (see fig1 , the bypass to the input switch of MUL).

10. As to claims 38-40, see the input switches at ADD and MUL in fig.3.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Morton (4,546,428) is cited for the background teaching of the bypass connection of an arithmetic unit with registers (see fig.11, see also col.8, lines 1-68, col.9, lines 1-43).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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